

# EXHIBIT 6

Application Serial No. 11/235,579  
Response to Office Action

Customer No. 01933

Attorney Docket No. 05644/LH

This paper is being submitted  
via EFS-Web on February 25, 2008

**IN THE UNITED STATES PATENT  
AND TRADEMARK OFFICE**

Applicant(s): Tomoyuki SHIRASAKI, et al.

Serial No. : 11/235,579

Confirm. No.: 3394

Filed : September 26, 2005

For : DISPLAY PANEL

Art Unit : 2814

Examiner : Long Pham

In the event that this Paper is late filed, and the necessary petition for extension of time is not filed concurrently herewith, please consider this as a Petition for the requisite extension of time, and to the extent not already paid, authorization to charge the extension fee to Account No. 06-1378. In addition, authorization is hereby given to charge any fees for which payment has not been submitted, or to credit any overpayments, to Account No. 06-1378.

**A M E N D M E N T**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

S I R :

This is responsive to the Office Action mailed October 23, 2007, the term for response to which is extended by one month by Petition filed concurrently herewith to expire on February 23, 2008 (Saturday), which is automatically extended to February 25, 2008.

**Amendments to the Claims** are set forth in the listing of claims which begins on page 2 of this paper. Claims 1 and 3-23 are amended, and claim 2 is canceled.

**Remarks** begin on page 12 of this paper.

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**Listing of Claims:**

1. (Currently Amended) A display panel comprising:

a transistor array substrate which ~~has~~ includes a plurality of pixels and ~~is formed by providing~~ comprises a plurality of transistors for each pixel, each of the ~~transistor having~~ transistors including a gate, a gate insulating film, a source, and a drain;

a plurality of interconnections which are formed to project ~~to from~~ from a surface of the transistor array substrate, and which are arrayed in parallel to each other;

a plurality of pixel electrodes ~~which are provided for the~~ plurality of pixels, respectively, the ~~each~~ pixel electrodes ~~being and~~ arrayed along the interconnections between the interconnections on the surface of the transistor array substrate ~~along the interconnections;~~

a plurality of light-emitting layers ~~each of which is~~ formed on ~~each the~~ pixel ~~electrode~~ electrodes, respectively; and

a counter electrode which is stacked on the light-emitting ~~layer~~ layers,

wherein said plurality of transistors for each pixel include a driving transistor, one of the source and the drain of which is connected to the pixel electrode, a switch transistor which makes a write current flow between the drain and the source of the

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25 driving transistor, and a holding transistor which holds a  
voltage between the gate and source of the driving transistor in  
a light emission period.

Claim 2 (Canceled).

3. (Currently Amended) A panel according to claim [[2]] 1,  
wherein said plurality of interconnections include at least one  
of a feed interconnection connected to the other of the source  
and the drain of at least one of the driving ~~transistor~~  
5 transistors, a select interconnection which selects at least one  
of the switch ~~transistor~~ transistors, and a common  
interconnection connected to the counter electrode.

4. (Currently Amended) A panel according to claim 3,  
wherein each of the light-emitting ~~layer~~ layers is formed between  
two of the feed interconnection, the select interconnection, and  
the common interconnection.

5. (Currently Amended) A panel according to claim 3,  
wherein said plurality of interconnections ~~are formed by arraying~~  
comprises a plurality of sets each including the feed  
interconnection, the select interconnection, and the common  
5 interconnection arrayed in an arbitrary order.

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**R E M A R K S**

Reconsideration of this application, as amended, is respectfully requested.

**ALLOWABLE SUBJECT MATTER**

The Examiner's allowance of claims 15-23 and the Examiner's indication of the allowability of the subject matter of claims 2-5 are respectfully acknowledged.

Claim 1 has been amended to incorporate the subject matter of claim 2, which has been canceled, and claim 3 has been amended to depend from amended independent claim 1 instead of from (now canceled) claim 2. In amending claim 1, the phrase "a switch transistor which supplies a write current" in original claim 2 has been changed to "a switch transistor which makes a write current flow." See, for example, Fig. 2 and page 41, lines 20-25 in the specification.

The claims have also been amended to make some minor grammatical improvements and to correct some minor antecedent basis problems so as to put them in better form for issuance in a U.S. patent.

No new matter has been added, and no new issues with respect to patentability have been raised.

Accordingly, it is respectfully requested that the amendments to the claims be approved and entered, and it is

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respectfully submitted that amended independent claim 1 and claims 3-14 depending therefrom are all in condition for immediate allowance, along with allowed claims 15-23.

THE DRAWINGS

It is respectfully requested that the Examiner complete item 10 of the Office Action Summary to confirm that the drawings filed with the application papers on September 26, 2005, have been accepted.

\* \* \* \* \*

Entry of this Amendment, allowance of the claims and the passing of this application to issue are respectfully solicited.

If the Examiner has any comments, questions, objections or recommendations, the Examiner is invited to telephone the undersigned for prompt action.

Respectfully submitted,

/Douglas Holtz/

Douglas Holtz  
Reg. No. 33,902

Frishauf, Holtz, Goodman & Chick, P.C.  
220 Fifth Avenue - 16<sup>th</sup> Floor  
New York, New York 10001-7708  
Tel. No. (212) 319-4900  
DH:iv

encs.